Study and Experimental Validation on Total Harmonic Distortion Reduction by Increasing Arm Inductance for Modular Multilevel Converter

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Abstract— This paper presents the effect of changing arm inductor for the modular multilevel converter (MMC) behavior in order to analysis the change in Total Harmonics Distortion (THD) for all MMC quantities including circulating current, upper arm current and voltage, lower arm current and voltage, and AC output voltage and current. The Operation principle, Circuit operation, and Converter equations are discussed first. Second, the multilevel modulation process for MMC is explained. Third, analysis of the Balancing of the submodules voltages based on sorting is carried out in this paper. For the reason that increasing arm inductor size could reduce the THD of MMC, this effect will be investigated in this paper. A new method to implement the submodules selection, which is the key technique for MMC for a wide range of a number of submodules per arm, is proposed and verified by the simulations. Analysis of the arm inductance value effect on MMC is carried out from many simulation results in this paper. Finally, the hardware design and software design of the prototype is presented to verify the arm inductor value effect on MMC experimentally. The experimental results are also documented in this paper.

Index Terms— Arm inductance effect on MMC.

1 Introduction

One of the important parts of MMC is the arm inductor. The inductor (Larm) for MMC is connected in the way of the DC transmission and in series with the converter as in Figure 1 for single phase. Arm inductor is placed to use its inductance in the electric circuit to surprise circulating current ripple to reduce higher harmonics as will be seen by simulation and experimentally. MMC was first presented as AC to AC and DC to AC converters, for high-power experimental prototypes [6]. MMC was presented as a cascaded converter based on cascading identical submodules [7]. The selection submodules have to be inserted or bypassed for each arm of the converter while maintaining each submodule capacitor voltage around its reference voltage, and phase arm modulation is an important aspect in the operation of the converter. The submodule, the heart of an MMC, has had its operation and circuit configuration explained before [1], [12], [13]. [12] simplifies the MMC by considering the sum of capacitor voltages in each arm instead of individual capacitor voltage. Different control approaches with various modulations were presented in [25] and [26] to investigate dynamic and required voltage balance of MMC topology. A number of applications such as voltage source converter-based HVDC transmission and back-to-back converter had been studied based on the use of MMC [21] and [27]. Also, in [28] and [29], high-voltage super-grids provided the possibility of using MMC in the configuration for multi-terminal HVDC. The modular topologies classification, presented in [7], does not rate the converter as a topology with many useful submodules for a DC system that can transmit up to 2200 KV. Power losses for both the converter and its submodules were evaluated in [30] and in [31], submodules losses were evaluated by utilizing different configurations for MMC. The effect of sampling frequency on total harmonics distortion in the operation of the converter was analyzed in [32]. Also, the effect of dead time in the submodule of the converter was considered in [33]. [34] presented minimization method of DC-link ripple, a mathematical model for the capacitor voltage variations, and improved voltage balancing control system for MMC in the converter topology [35]. Arm inductance and submodule capacitance can be calculated in different methods as in [37], [38], and [39]. Also, smoothing reactor for HVDC systems has been evaluated exactly [40] and approximated [41]. Transmitting power 10,000 MW and distance up to 3000 km with ± 1100 kV DC is consider economic, efficient, mature technology [6] and [42]. The DC bus voltage of UHVDC transmission system determines the number of submodules per arm. Therefore, with 2200 KVDC ([6], [42], [43]), each converter arm consists of a large number of submodules. The ripple shall be within limits up to 10% of the direct current value [36]. Arm inductor can be with value of inductance up to 1.5 H, While for back-to-back systems values is varying from high of 200mH to a low of 12mH [37], [39]. Also, it can smooth the circulating current by reducing the ripple in the direct current in order to prevent the current becoming discontinuous at light load. Moreover, it can be used to decrease harmonic output voltages and current in the MMC system. More importantly, the decreasing THD becomes the major concern for sensitive industry and HVDC applications. The importance of this paper that offering for industry applications either medium or high voltages two choices to reduce THD either by a large number of submodules per arm or increasing arm inductance instead.

2 Operation Principles and Converter Equations

Figure 1 illustrates a final single-phase MMC circuit with its submodule. Since the capacitors are not guaranteed to provide constant voltage when connected to a circuit, this brings some problems. If a capacitor is inserted in the arm, its voltage varies according to the direction of the current. The simplest and accurate solution is to use the effect that charges and discharges the capacitors actively in the converter modulation

itself through a specific algorithm to be explained in detail later in this paper. However, capacitor voltages are still inconstant, something which could cause current transient due to unequal voltages between the legs. For this reason, inductances are also placed in each arm. The heart of the MMC is the submodule and its basic half-bridge scheme appears in Figure 1.

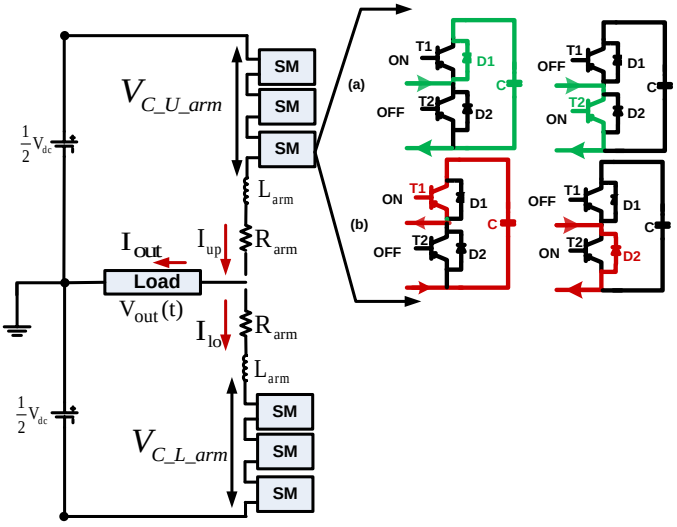


Figure 1. Single-phase MMC circuit and its submodule ((a) Positive and (b) negative current flow inside an MMC submodule

Table 1 shows switching states for the submodule. In the latter situation and based on the proposed algorithm, the capacitor maintains its state of charge and its voltage remains unchanged. Using switching states in Table 1, it is possible to control each of the submodules separately.

TABLE 1
SWITCHING STATES FOR EACH SUBMODULE

T1	T2	D1	D2	Current direction	Capacitor state	Output voltage
OFF	ON	OFF	OFF	Iarm>0	Uncharged (bypassed)	0
OFF	OFF	OFF	ON	Iarm<0	Uncharged (bypassed)	0
OFF	OFF	ON	OFF	Iarm>0	Charging	VC
ON	OFF	OFF	OFF	Iarm<0	Discharging	VC

To explain how the proposed PWM algorithm works for MMC circuit, a specific example will show how to generate a voltage waveform. In this example, the number of submodules per each leg will be 4; the converter will convert DC to AC with the 5-level waveform (n=N+1; where n number of output voltage level), which will be explained in detail. The voltage across each capacitor can be given as in (1):

$$V_C = \frac{V_{dc}}{N} = \frac{V_{dc}}{4}\ V. \qquad (1)$$

V_{dc} is DC bus voltage, and assuming the submodule selection process is effective, the submodule capacitors within a converter arm can be assumed to be equally charged. This is possible with a switching frequency high enough to allow the modulator to act even on very small disturbances in this balance. It will be proven later that these assumptions can apply for a small number of submodules. Figure 1 shows an equivalent electrical circuit for one phase leg of MMC and Table 2 shows MMC parameters definitions.

Let the converter consist of N submodules per arm. In general, each arm is controlled by an insertion index x, which is defined such that x = 0 means that all N submodules in the arm are bypassed, while x = 1 means that all N submodules in the arm are inserted. In the former case, the current is flowing through the arm will not pass through any capacitor, so the equivalent capacitive arm impedance is zero. In the latter case, the arm current will meet N capacitors connected in series, making the equivalent capacitance of the arm C/N. If each submodule capacitor has capacitance C, the effective capacitance of the one arm is given by (2):

TABLE 2
MMC PARAMETER DEFINITIONS

C	Submodule capacitance
x	Insertion index
I_{up}	Upper arm current
I_{lo}	Lower arm current
Icir	Circulating current
I_{out}	Output phase current
xU	Insertion indices of the upper arm
xL	Insertion indices of the lower arm
$V_{C\,U\,arm}(t)$	Total upper arm capacitor
$V_{C\,L\,arm}(t)$	Total lower arm capacitor
V_{dc}	DC bus
V_{out}	Output phase voltage

$$C_{arm} = \frac{C}{N.x}. \qquad (2)$$

Naming the upper and lower arm currents I_{up} and I_{lo} respectively, and defining their polarities as illustrated on Figure 1, the output phase current is calculated as their sum in (3).

$$I_{out} = I_{up} - I_{lo}. \qquad (3)$$

The output phase current is assumed to be equally shared by both upper and lower arm. However, and as mentioned in previous paragraphs, there is a deviation from this ideal condition since part of the current passes through the series-connected arms and the DC source. Let this circulating current be called I_{cir} as in (4).

$$\left.\begin{aligned} I_{up} &= I_{cir} + \frac{I_{out}}{2} \\ &\vdots \\ I_{lo} &= I_{cir} - \frac{I_{out}}{2} \end{aligned}\right\} \xrightarrow{\sum} I_{cir} = \frac{I_{up} + I_{lo}}{2}. \qquad (4)$$

In a three-phase system, $I_{cir}=(1/3)I_{dc}$ and in a single phase system, $I_{cir}=I_{dc}$.

Defining xU and xL as the insertion indices of the upper and the lower arm respectively, the following equation is derived:

$$V_{out} = \frac{x_L V_{C\_L\_arm} - x_U V_{C\_U\_arm}}{2} - \frac{R_{arm}}{2} I_L - \frac{L_{arm}}{2} \frac{dI_L}{dt} \qquad (5)$$

Where V_{out} the output phase voltage, by solving the last two equations, the equivalent voltage for the external load connected to the AC terminal becomes, and $V_{C\_U\_arm}(t)$ and $V_{C\_L\_arm}(t)$ are total upper arm capacitor and total lower arm capacitor respectively.

It is obvious from (4) that upper arm current generates the positive half cycle of the output AC current while lower arm current generates its negative half cycle. Also, from (5), it is obvious that upper arm voltage generates the negative half cycle of output AC voltage while lower arm voltage generates its positive half cycle of the output AC voltage as will be proved by computer simulation and experimental prototype.

3 Proposed PWM Algorithm

3.1 Reference arm voltage for N submodules

The proposed PWM algorithm of MMC is based on the equalization of the inserted submodules for one arm with the bypassed submodules for the other arm. First, the operation of MMC as n (N+1) level converter is discussed. The principle is that in each instant, N submodules are inserted and N submodules bypassed for the whole leg. Let NU be the number of submodules inserted in the upper arm and NL the number of submodules inserted in the lower arm. Accordingly, the AC terminal can take N+1 different potentials when the number of inserted modules varies between 0 and N. A sinusoidal reference is applied to the modulator, which is then converted into a varying insertion index for each arm as defined by (6), where ωN is the angular frequency of the output voltage.

$$m(t) = N * \hat{m} \cos(\omega_N t) \qquad (6)$$

m is the maximum value for modulation index, which is 1. The main target from this process getting a number of inserted submodules for both arms with keeping the condition of this method mentioned above. Therefore, equation (6) will split into two equations (7), leading to (8) and (9):

$$\left.\begin{aligned} N_{U,bypassed} &= N - N_{L,bypassed} = N_{L,inserted} \\ N_{U,inserted} &= N - N_{L,inserted} = N_{L,bypassed} \end{aligned}\right\} \longrightarrow \qquad (7)$$

$$N_U = \frac{N - m(t)}{2} \qquad (0 < N_U \leq N) \qquad (8)$$

$$N_L = \frac{N + m(t)}{2} \qquad (0 < N_L \leq N) \qquad (9)$$

This step is considered a starting point for indirect PWM as can be seen later. Figure 2 (a) shows m(t) and a number of inserted submodules for both upper and lower arms in a sinusoidal waveform.

3.2 Flooring arms voltages references

Since the numbers of inserted or bypassed submodules for both arms are real, positive integers, flooring both sine waves of upper and lower arms is necessary. Flooring value (a) is choosing (a) to the nearest integer in the direction of negative infinity, while ceiling value (a) is choosing (a) to the nearest integer in the direction of positive infinity. For example, flooring value for 0.5 is 0 and flooring value for 1.99 is 1. Figure 2 (b) shows inserted submodules for both arms after flooring (green signal is N before flooring and red signal is N after flooring).

3.3 References arms voltages and carrier signals modulator

At the same time as the last step, the reference signals for both upper and lower arms are modulated with a carrier signal and a switching frequency for the switches as seen in Figure 2(c). The modulator will modulate both signals to the waveform in Figure 2(d) for both upper and lower arms respectively in a process which aims to create a signal which matches an assigned reference, by averaging the number of inserted submodules between a floor and a ceiling number in every sampling period. This process determines the inserted submodules for both upper and lower arms and the exact instants of the switching actions. Figure 2(d) shows inserted submodules for upper and lower arms at the same time, with the number of inserted submodules in one arm equal to the number of bypassed submodules (N-NL_inserted) in the other arm, which achieves balancing voltages between the upper arm and lower arm across the AC terminal.

A sinusoidal waveform in the output can, therefore, be achieved by varying the number of the submodules in the upper and lower arm with a sinusoidal manner. Since the voltage of each arm is not continuous but varies with the switching of the submodules, the selection of the submodules and PWM method applied to the converter affects its operation and output waveforms. The two arms that comprise the phase-leg of the converter can be modulated either simultaneously or independently.

The number of submodules to insert or bypass was found by comparing voltage reference with carrier waves. The next step, the selection of submodules, can be based on their capacitor voltage measurements. When the multivalve current direction is known, it can be predicted whether the capacitor will charge or discharge when inserted. This information is used to insert or bypass submodules closest to the range limits

and thus keep the capacitors voltages balanced. A positive current will charge the inserted capacitors, while a negative current will discharge them. That leads to submodules selection.

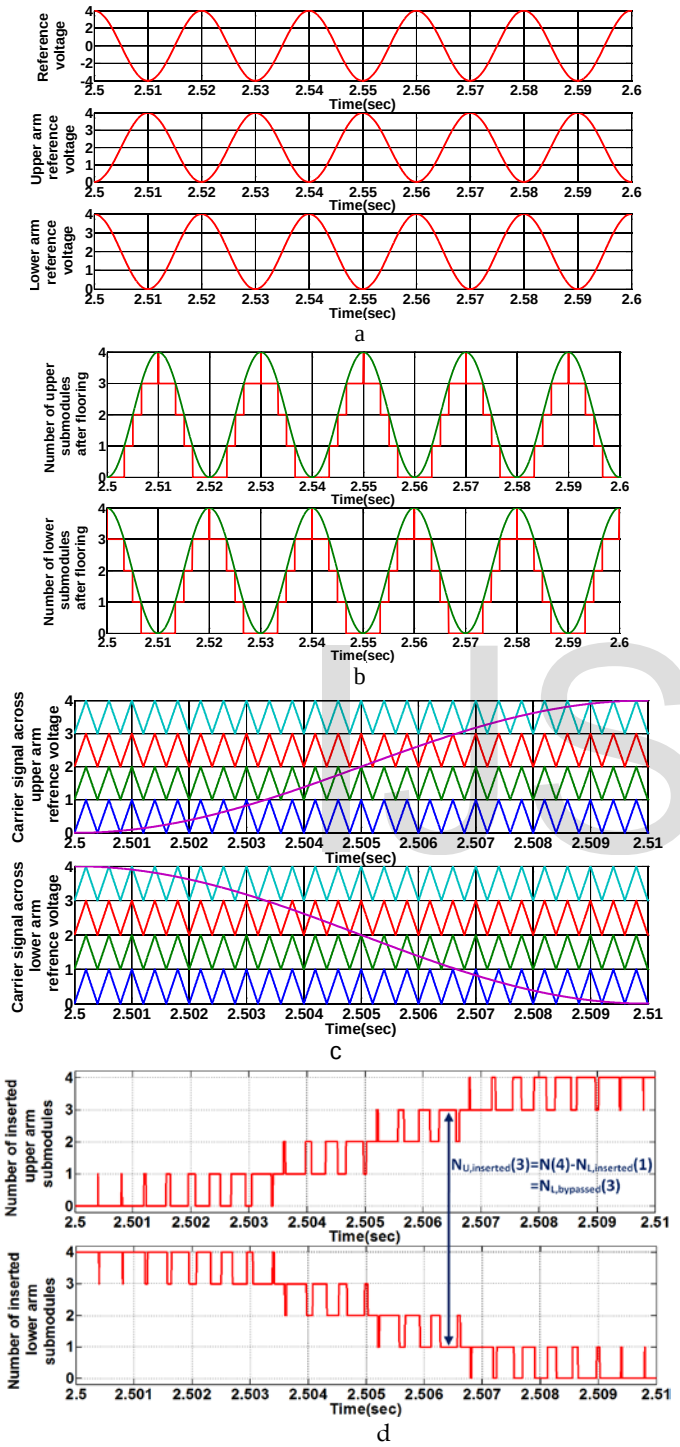


Figure 2 PWM signal and its generated number of submodules

a. Reference voltage, the number of inserted submodules for both arms in continuous mode.
b. Number of upper and lower submodules after flooring.
c. Reference signals for both upper and lower arms across carrier signal.
d. Number of inserted submodules for upper and lower arms.

3.4 Submodules selection

To maintain the individual voltage of each submodule around its reference voltage takes an active balancing method. The voltage of each individual submodule together with the arm current needs to be measured and available in the voltage-balancing algorithm. The voltage-balancing algorithm selects the submodules in each of the arms of the converter based on the relative voltage values of all the arm submodules and direction of the arm current. Ascending or descending capacitor voltages are required to be used for balancing algorithm. The next submodule that switches in the arm is selected based on the direction of the current and the sorted voltages so that

When the arm current is positive (iarm > 0) and the modulation process method requires the addition of one submodule in the arm, the balancing algorithm will select the submodule with the lowest voltage that is not connected to be inserted into the arm.

If the arm current is positive (iarm > 0) and the modulation process method requires the subtraction of one submodule in the arm, the balancing algorithm will select the submodule with the highest voltage that is connected to the arm to be bypassed and removed from the arm.

If the arm current is negative (iarm > 0) and the modulation process method requires the addition of one submodule in the arm, the balancing algorithm will select the submodule with the highest voltage that is not connected to the arm to be inserted to the arm.

If the arm current is negative (iarm < 0) and the modulation process method requires the subtraction of one submodule in the arm, the balancing algorithm will select the submodule with the lowest voltage that is connected to the arm to be bypassed and removed from the arm.

The capacitor voltage of the submodule will not change when the submodule is not connected to the arm of the converter; it will remain at the level it was before it was removed from the arm of converter. The voltage balancing algorithm uses the data coming from the modulation process, upper and lower arms currents, and upper and lower arms sorting voltages. Figure 3 shows the proposed PWM algorithm sorting both arms voltages. The main aim of the selection process is to maintain the voltages of the capacitors close to the reference values. This is accomplished during the whole cycle of the waveform and the capacitors' actual voltages drift from their reference value within this cycle due to the load current coming from upper and lower arms currents. Moreover, the algorithm considers the actual values for capacitor voltages coming from voltages measurements after sorting them in the selection of the submodules, but their relative voltage relates to the remaining submodules in the arm. In some cases, the submodule selected to be inserted into the arm of the converter according to the logic of the algorithm will further deviate from the reference voltage. The balancing of the submodule is not an instantaneous process and balancing around the reference occurs over the fundamental period.

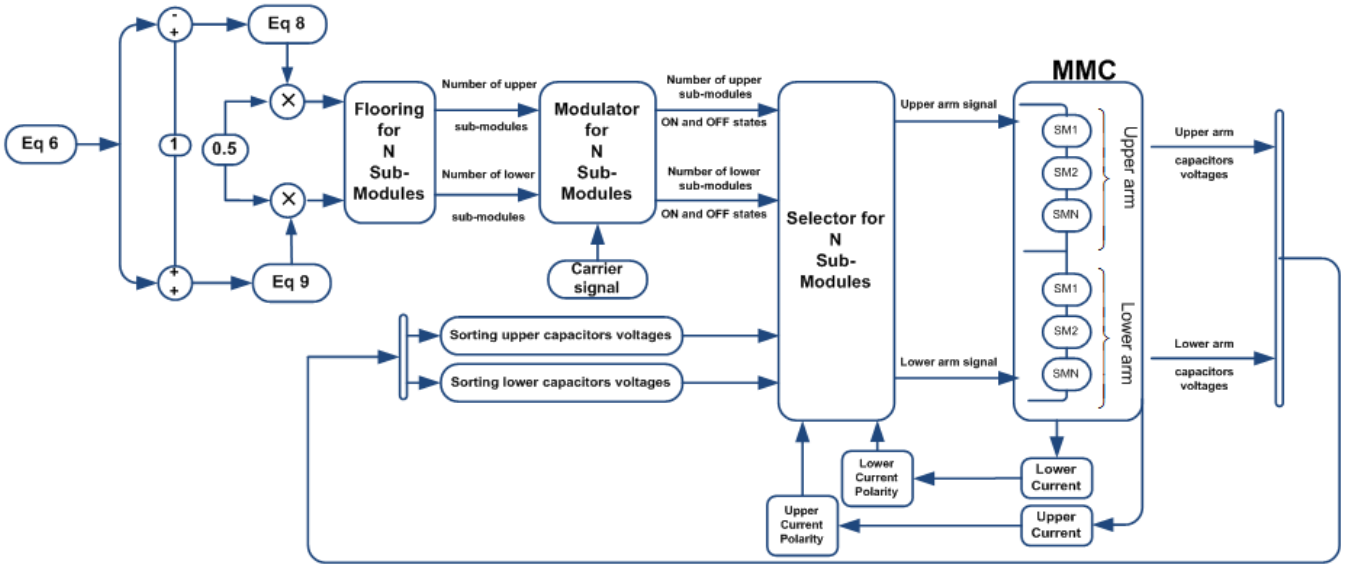


Figure 3. Proposed PWM algorithm with sorting voltage for MMC

4. SIMULATION RESULTS

Since increasing the arm inductor is used to suppress the circulating current to be stable. The stability of circulating current tends to stability of submodule voltage in the arm. Upper arm voltage and lower arm voltage will have less THD when the fluctuation of the capacitor voltage is going to be less and less. 50-level MMC had been chosen to analyze the behavior of MMC with different values of arm inductors. Table 2 shows figures 4(d) and 5(d).

the simulation results for MMC 50-level at different values of arm inductor with the same DC bus and all parameters compared with calculated value(13.1mH). As can be seen from figure 4(a) and 5(a) output voltage and current for MMC at 85mH is smoother that at 13.1mH and as values from Table 2 the THD was reduced almost 90% from 5.05% to 2.8%. Moreover, it is obvious that the circulating current ripple has been suppressed from 63.96% to 14.84% and this difference is very clear from circulating current waveforms as can be seen in

TABLE 3

THE SIMULATION RESULTS FOR MMC 50-LEVEL AT DIFFERENT VALUES OF ARM INDUCTOR WITH THE SAME DC BUS AND ALL PARAMETERS

Inductor size (mH) For 25 level at 9.3mF	Output Voltage		Output Current		Upper arm current		Lower arm current		Capacitor voltage		Circulating current	
	THD%	Max. Value (KV)	THD%	Max. Value (A)	THD%	DC component (A)	THD%	DC component (A)	Voltage ripple	DC component (V)	Current ripple %	DC component (A)
13.1	5.05	2.414	0.57	92.13	15.19	21.7	15.2	21.7	8.8	207.1	63.96	21.7
15	4.92	2.41	0.56	91.77	13	21.5	13	21.5	8.5	206.1	54.14	21.5
20	4.61	2.38	0.5	90.81	9.41	21	9.4	21	7.63	205.9	40.24	21
25	4.34	2.35	0.46	89.8	7.42	20.6	7.42	20.6	7.8	205.97	32.1	20.59
30	4.1	2.33	0.44	88.7	6.2	20.1	6.2	20.1	7.4	205.9	27.1	20.1
35	3.93	2.3	0.4	87.7	5.3	19.6	5.3	19.6	7.4	205.98	23.43	19.63
45	3.6	2.24	0.37	85.5	4.1	18.65	4.1	18.65	7.2	205.9	18.8	18.65
55	3.35	2.18	0.33	83.2	3.4	17.7	3.4	17.7	7.1	205.9	15.8	17.7
65	3.1	2.12	0.3	80.9	2.9	16.7	2.9	16.7	6.9	205.6	13.4	16.7
75	2.9	2.06	0.28	78.6	2.58	15.75	2.58	15.75	6.7	205.8	12.7	15.75
85	2.8	1.99	0.26	76.25	2.3	14.84	2.3	14.84	6.5	205.79	11.4	14.84

Figures from 4(a) to 4(d) show the simulation results for

MMC 50-level at calculated value of the arm inductor 13.1mH, V_{dc} = 5000 V, arm resistor = 0.5ohm, load inductor = 25mH, load resistor = 25, ohm, power factor =0.9540, and submodule capacitor= 0.0185 F.

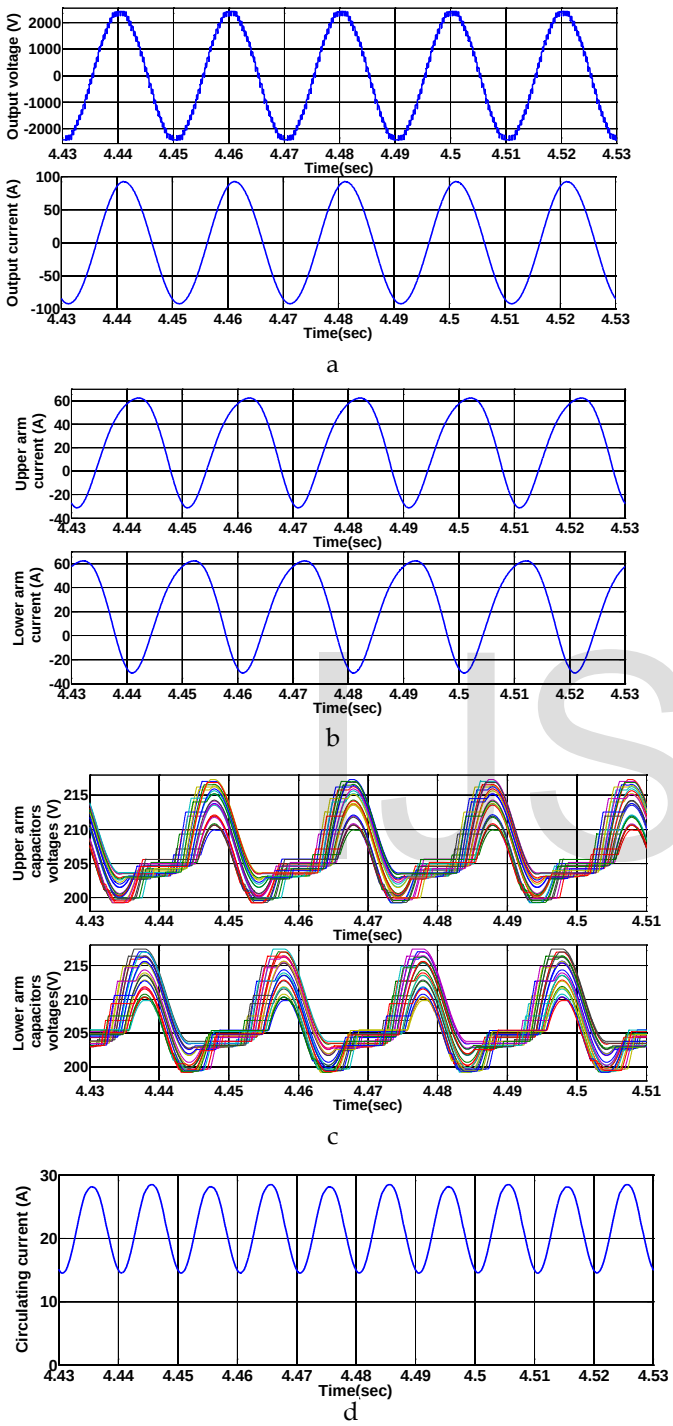


Figure 4. Simulation results for AC for 25- level MMC at arm inductor 13.1 mH

a. the output voltage and current
b. upper and lower arms currents
c. intermediate capacitors upper and lower arms and
d. circulating current

Figures 5(a) to 5(b) show the simulation results for MMC 50-level at eight times of inductance value of the arm inductor (40mH) without change for other parameters.

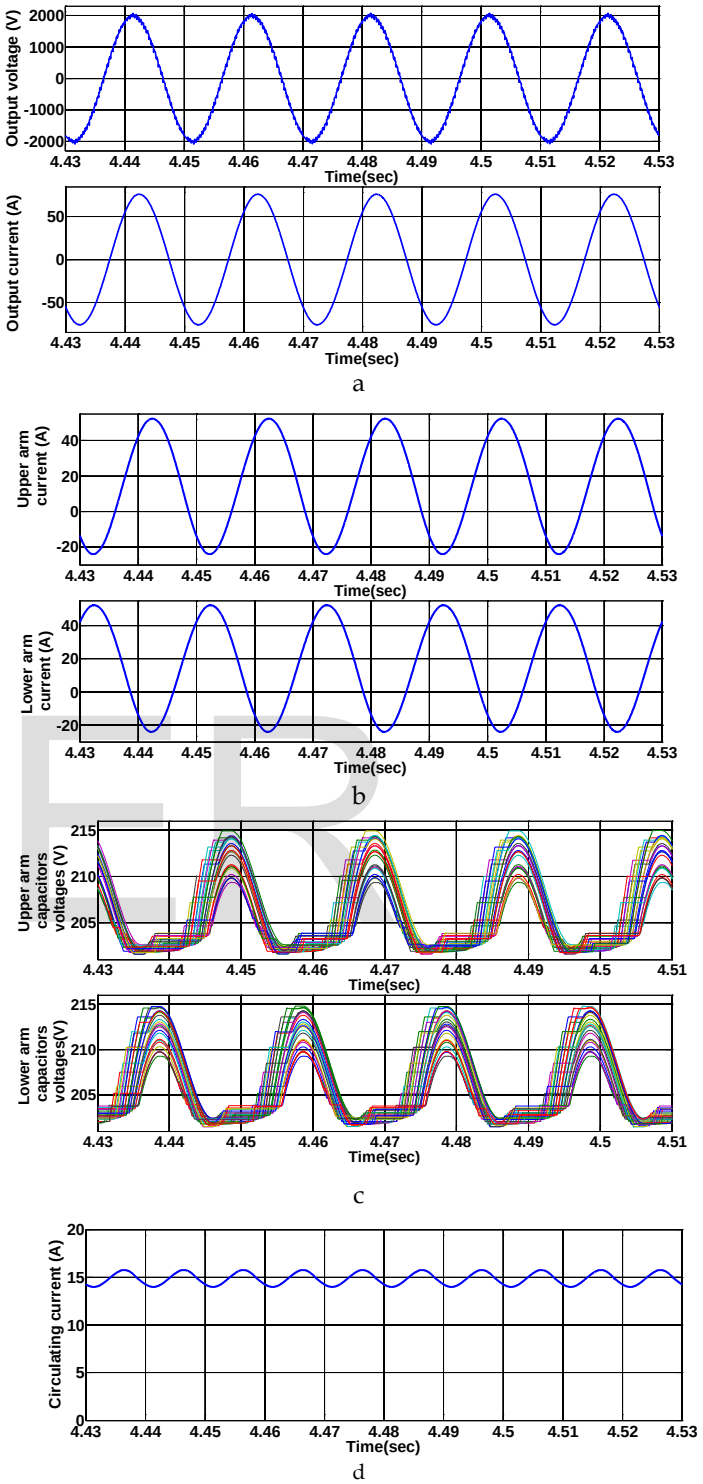
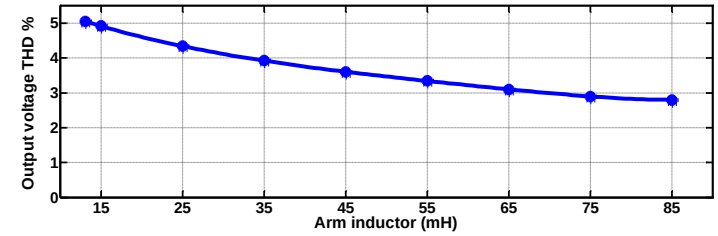


Figure 5. Simulation results for AC for 25- level MMC at arm inductor 85 mH

a. The output voltage and current
b. upper and lower arms currents
c. intermediate capacitors upper and lower arms and
d. circulating current

Figure 6(a) shows the relationship between arm inductor and output voltage THD, figure 6(b) shows the relationship

between arm inductor and maximum output voltage, and figure 6(c) shows the relationship between arm inductor and circulating current ripple. As expected and can be seen from Table 2, THD for output voltage and current, THD for upper and lower arms current, circulating current ripple can be reduced by increasing the value of arm inductor.



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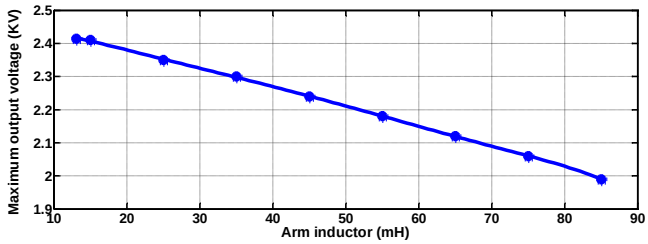

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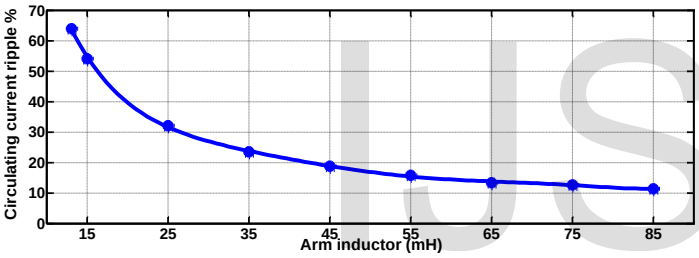

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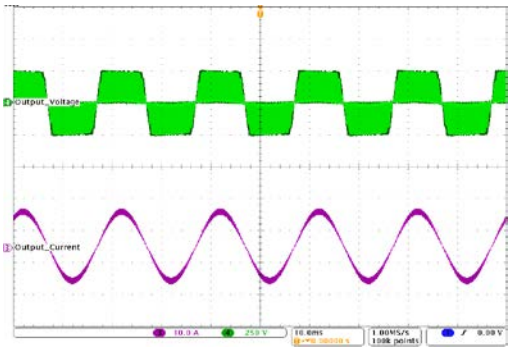
Figure 6. The relationships of arm inductor with
a. THD output voltage
b. Maximum output voltage
c. Circulating current ripple

5. EXPERIMENTAL RESULTS

The proposed modulation for the MMC is also verified on a phase-leg experimental prototype with two submodules per arm. The specifications of the laboratory prototype are given in Table 3. The results, which are given below, correspond to single-phase operation with 3kHz switching frequency. Figure 7(a) shows the output voltage of the 3-level modulation concept and output phase current. Figure 7(b) shows upper and lower arm current generating output current and Figure 7(c) shows upper and lower arm voltages generating output voltage.

TABLE 4
MMC laboratory prototype specifications

Parameters	Values
DC voltage	500 V
R_{load}	20 Ω
L_{load}	2.2 mH
Submodules capacitance	2.2 mF
Arm inductance	3.5 mH
Arm resistance	0.1 Ohm
Number of submodules per arm	2
Submodules voltage	250 V
Number of output level	3
Reference frequency	50Hz
Carrier frequency	3KHz



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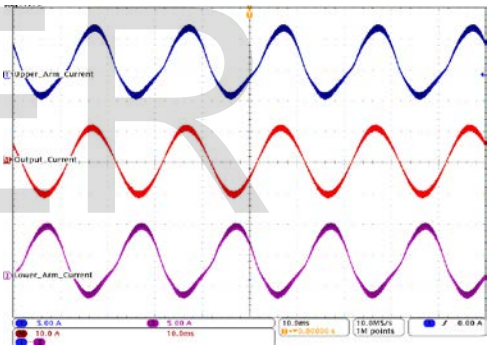

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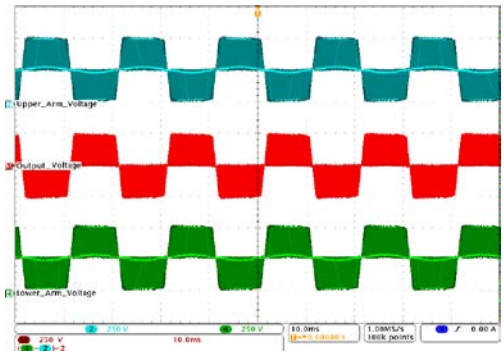

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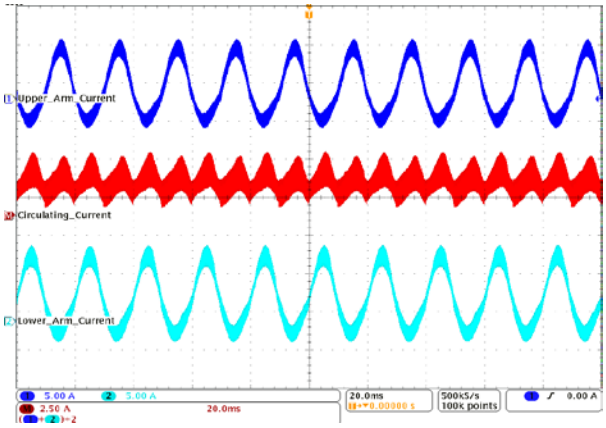
Figure 7. Experimental results for 3-level MMC
a. Three-level phase-voltage and load current.
b. Currents through the upper (top) arm, lower (bottom) arm and output current (middle) of the MMC.
c. Upper arm voltage (top), lower arm voltage (bottom) and output voltage (middle) of the MMC.

Since the change in output voltage with increasing arm induc-

tance is invisible experimentally with small number of output voltage level. Therefore, circulating current waveforms with 10 ms period were recorded at different values of arm inductance. Figures 8(a) to 8(d) show the suppression of circulating current with increasing arm inductor up to four times. It is obvious that circulating current is going to be flat more with increasing arm inductance.



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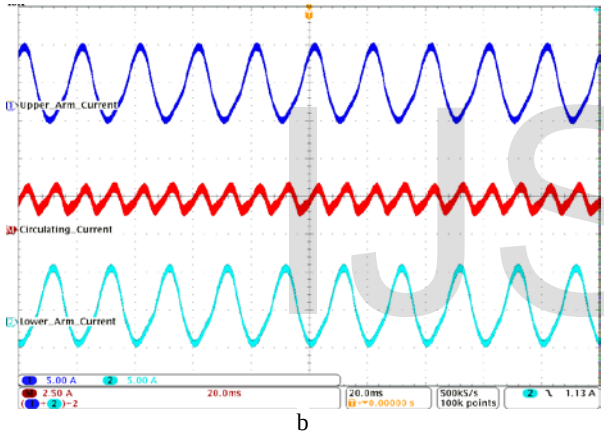

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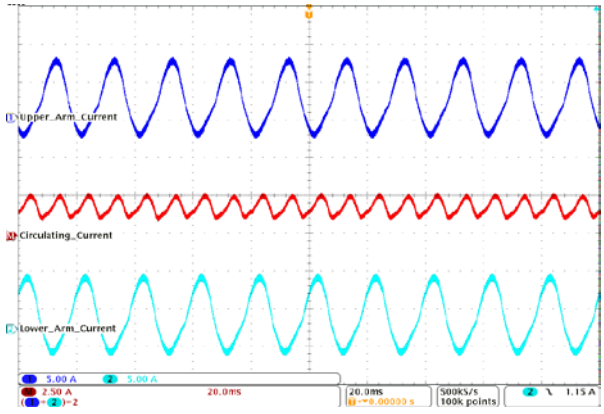

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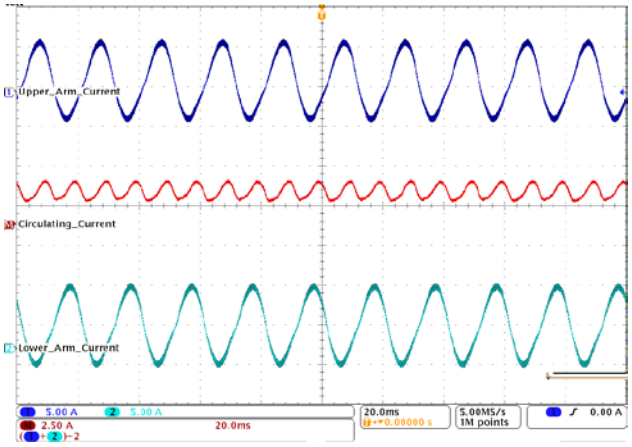

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Figure 8. Experimental Results for Currents through the upper (top) arm, lower (bottom) arm and output current (middle) of the MMC at

a. 3.5mH arm inductor
b. 7.2 mH arm inductor
c. 10 mH arm inductor
d. 14.1 mH arm inductor

6. Conclusion

This paper described the effectiveness of arm inductor on MMC THD for all quantities including maximum output voltage and current, circulating current and capacitor voltage ripples. Also, the study presented THD deduction by increasing arm inductance instead of increasing number of submodules per arm offering more options to reduce the cost. The relationships of arm inductor with THD output voltage, maximum output voltage, circulating current ripple and submodule capacitor voltage ripple were presented. It is obvious that increasing the arm inductance leads to stabilize the circulating current and capacitor voltage which leads to reduce THD for the output voltage and current. The proposed PWM control comes to fulfill the requirements of UHVDC bus voltage in this paper with many contributions. Since there will be demand for UHVDC in the next years. The proposed method works with low switching frequency for UHVDC systems, which will decrease converter losses. Moreover, for MMC itself the proposed method offers simple numerical algorithm for MMC topology that can be used with large or small number of submodules per arm either experimentally or by simulation. Selection process for inserting or bypassing submodules guarantees capacitors voltages around the reference voltage (Vdc/N) with voltage ripple less than 7% even for large number of submodules per arm. More converter stability can be achieved by equal sharing of currents from both arms to the load. Overall, the proposed PWM allows MMC to be used with large scale of power transmission either HVDC systems or large scale of solar energy and also can be used for large motors control. In this paper, the prototype hardware, the implementation and experimental results of the effectiveness of arm inductor on MMC behavior is discussed and evaluated in order to bring agreement with simulation results.

REFERENCES

[1] A. Lesnicar, R. C. Marquadt., "A new modular voltage source inverter topology," Institute of Power Electronics and Control, Universität der Bundeswehr München, Werner-Heisenberg-Weg 39, 85577 München, Germany, 2004.

[2] Grain Philip Adam, Stephen Jon Finney, and Barry Wayne Williams, "Hybrid converter with ac side cascaded H-bridge cells against H-bridge alternative arm modular multilevel converter: steady-state and dynamic performance," Generation, Transmission & Distribution, IET , vol. 7, no. 3, pp. 318 - 328, Mar. 2013.

[3] Quanrui Hao, Guo-Jie Li, and Boon-Teck Ooi, "Approximate model and low-order harmonicn reduction for high-voltage direct current tap based on series single-phase modular multilevel converter," Generation, Transmission & Distribution, IET, vol. 7, no. 9, pp. 1046 - 1054, Sep. 2013.

[4] Hendrik Fehr, Albrecht Gensior, and Marcus M¨uller , "Analysis and Trajectory Tracking Control of a Modular Multilevel Converter," IEEE Transaction on Power Electronics, vol. 30, no. 1, pp. 398–407, Jan. 2014.

[5] Can Wang, Quanrui Hao, and Boon-Teck Ooi, " Reduction of low-frequency harmonics in modular multilevel converters (MMCs) by harmonic function analysis," Generation, Transmission & Distribution, IET, vol. 8, no. 2, pp. 328 - 338, Feb. 2014.

[6] M. Glinka, "Prototype of multiphase modular-multilevel-converter with 2MWpower rating and 17-level-output-voltage," in Power Electronics. Specialist Conf., PESC, pp. 2572–2576, 2004.

[7] Hirofumi Akagi, "Classification, terminology and application of the modular multilevel cascade converter (MMCC)," IEEE Transaction on Power Electronics., vol. 26, no. 11, pp. 3119–3130, 2011.

[8] Sawata R. Deore, Pranav B. Darji and Anil M. Kulkarni, "Switching function analysis of half- and full-bridge modular multi-level converters for HVDC applications," Generation, Transmission & Distribution, IET, vol. 7, no. 11, pp. 1344–1365, Nov. 2013.

[9] Can Wang, Quanrui Hao and Boon-Teck Ooi, "Reduction of low-frequency harmonics in modular multilevel converters (MMCs) by harmonic function analysis," Generation, Transmission & Distribution, IET, vol. 8, no. 2, pp. 328–338, Feb. 2014.

[10] Elisabeth N. Abildgaarda and Marta Molinas, "Modelling and Control of the Modular Multilevel Converter (MMC),. Technoport 2012 - Sharing Possibilities and 2nd Renewable Energy Research Conference (RERC2012), vol. 20, pp. 227–236, 2012.

[11] Xiaoqian Lia, Qiang Songa, Wenhua Liua, Qi Lia, Hong Raob and Shukai Xu, "Zero-sequence voltage injection control scheme of modular multilevel converter supplying passive networks under unbalancedload conditions," Electric. Power System Research., Nov. 2011.

[12] Lennart Harnefors, Antonios Antonopoulos, Staffan Norrga, Lennart Ängquist, and Hans-Peter Nee, "Dynamic Analysis of Modular Multilevel Converters," IEEE Transactions on Industrial Electronics, vol. 60, no. 7, pp. 2526–2537, Jul. 2013.

[13] Georgios S. Konstantinou and Vassilios G. Agelidis, "Performance evaluation of half-bridge cascaded multilevel converters operated with multicarrier sinusoidal PWM techniques," 4th IEEE Conf. on Industrial Electronics and Applications, pp. 3399–3404, May 2009.

[14] Daniel Siemaszko, "Fast Sorting Method for Balancing Capacitor Voltages in Modular Multilevel Converters," IEEE Transaction on Power Electronics, vol. 30, no. 1, pp. 463–470, Mar. 2014.

[15] Maryam Saeedifard and Reza Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," IEEE Transaction on Power Delivery, vol. 25, no. 4, pp. 2903-2912, 2010.

[16] Josep Pou, Salvador Ceballos, Georgios Konstantinou, Vassilios Agelidis, Ricard Picas, and Jordi Zaragoza, "Circulating Current Injection Methods Based on Instantaneous Information for the Modular Multilevel Converter," IEEE Transaction on Industrial Electronics vol. pp 1-11, no. 99, pp. 1, Jul. 2014.

[17] Antonios Antonopoulos, Lennart Ängquist, Lennart Harnefors, Kalle Ilves and Hans-Peter Nee, "Stability analysis of modular multilevel converters with open-loop control," Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE, pp. 6316–6321, Nov. 2013.

[18] B. R. Baroni, M. A. Mendes, P. C. Cortizo, A. C. Lisboa and R. R. Saldanha, "Application of modular multilevel converter for HVDC transmission with selective harmonics," Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE, pp. 6195–6200, Nov. 2013.

[19] Hans Bärnklau, Albrecht Gensior and Joachim Rudolph, "A Model-Based Control Scheme for Modular Multilevel Converters," IEEE Transactions on Industrial Electronics, vol. 60, no. 12, Dec. 2013.

[20] Kalle Ilves, Antonios Antonopoulos, Staffan Norrga and Hans-Peter Nee, "Steady-State Analysis of Interaction Between Harmonic Components of Arm and Line Quantities of Modular Multilevel Converters," IEEE Transaction on Power Electronics vol. 27, no. 1, pp. 57–68, Jun. 2012.

[21] Steffen Rohner, Steffen Bernet, Marc Hiller and Rainer Sommer, "Modulation, losses and semiconductor requirements of modular multilevel converters," IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2633-2642, Jul. 2010.

[22] Minyuan Guan, and Zheng Xu, "Modeling and Control of a Modular Multilevel Converter-Based HVDC System Under Unbalanced Grid Conditions," IEEE Transaction on Power Electronics vol. 27, no. 12, pp. 4858–4867, Dec. 2012.

[23] Antonios Antonopoulos, Lennart A¨ ngquist, and Hans-Peter Nee, "On dynamics and voltage control of the modular multilevel converter," Power Electronics and Applications, 2009. EPE '09. 13th European Conference on, pp. 1–10, Sep. 2009.

[24] Georgios Konstantinou, Mihai Ciobotaru and Vassilios Agelidis, "Operation of a modular multilevel converter with selective harmonic elimination PWM," Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on, pp. 999–1004, Jun. 2011.

[25] Kalle Ilves, Antonios Antonopoulos, Staffan Norrga and Hans-Peter Nee, "A new modulation method for the modular multilevel converter allowing fundamental switching frequency," IEEE Transactions on Power Electronics, vol. 27, no. 8, pp. 3482–3494, Jan. 2012.

[26] Antonios Antonopoulos, Kalle Ilves, Lenart Ängquist, Hans-Peter Nee, "On interaction between internal converter dynamics and current control of high-performance high-power AC motor drives with modular multilevel converters" Energy Conversion Congress and Exposition (ECCE), pp. 4293–4298, Sep. 2010.

[27] Georgios S. Konstantinou Mihai Ciobotaru, and Vassilios G. Agelidis , "Analysis of multi-carrier PWM Methods for back-to-back HVDC systems based on modular multilevel converters," IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society, pp. 4238–4243, Nov. 2011.

[28] Noman Ahmed, Arif Haider, Dirk Van Hertem, Lidong Zhang and Hans-Peter Nee, "Prospects and challenges of future HVDC super-grids with modular multilevel converters," Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on, pp. 1–10, Sep. 2011.

[29] Xiaodong Yang, Chengyong Zhao, Jing Hu, Jing Wang, and Liu Yang , "Key technologies of three-terminal DC transmission system based on modular multilevel converter," Electric Utility Deregulation and Restructuring and Power Technologies (DRPT), 2011 4th International Conference on, pp. 499–503, Jul. 2011.

[30] Qingrui Tu, and Zheng Xu, "Power losses evaluation for modular multilevel converter with junction temperature feedback," Power and Energy Society General Meeting, 2011 IEEE, pp. 1–7, Jul. 2011.

[31] Tomas Modeer, Hans-Peter Nee and Staffan Norrga, "Loss comparison of different sub-module implementations for modular multilevel converters in HVDC applications," Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference, pp. 1–10, Sep. 2011.

[32] Qingrui Tu, and Zheng Xu, "Impact of sampling frequency on harmonic distortion for modular multilevel converter," IEEE Transaction on Power Delivery, vol. 26, no. 1, pp. 298–306, 2011.

[33] Zixin Li, Yaohua Li, Ping Wang, Haibin Zhu, Zunfang Chu, and Song Wang , "Improving the performance of modular multilevel converter by reducing the dead time effect," Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference, pp. 1–10, Sep. 2011.

[34] Abd Almula G. M. Gebreel 'POWER CONVERSION FOR UHVDC TO UHVAC BASED ON USING MODULAR MULTILEVEL CONVERTER' , P.hD Dissertation, ohio State university , 2015

[35] Shengfang Fan, Kai Zhang, Jian Xiong, and Yaosuo Xue, "An Improved Control System for Modular Multilevel Converters with New Modulation Strategy and Voltage Balancing Control," IEEE Transaction on Power Electronics, vol. 30, no. 1, pp. 358–371, Jan. 2015.

[36] Abd Almula G. M. Gebreel 'simulation and implementation of two level and three-level inverters by matlab and RT-lab' , master thesis , ohio State university , 2011

[37] Abd Almula G. M. Gebreel, Longya Xu 'Power quality and total harmonic distortion response for MMC with increasing arm inductance based on closed loop-needless PID controller' , Electric Power Systems Research, Vol. 133, PP 281-291, April 2016

[38] Abd Almula G. M. Gebreel, Longya Xu 'Numerical Analysis and Simulation Implementation for SVPWM Based on a New Region Segment Configuration Method' , International Journal of Scientific & Engineering Research, Vol. 6, No. 3, PP 614-621, April 2015.

[39] Abd Almula G. M. Gebreel, Longya Xu 'Power Conversion for UHVDC to UHVAC Based on Using MMC with Large Scale of Output Voltage Level' , International Journal of Electrical and Electronics Research, Vol. 4, No. 3, PP 125-139, April 2016.

[40] Abd Almula G. M. Gebreel, Longya Xu 'DC–AC Power Conversion Based on Using Modular Multilevel Converter With Arm Energy Approximation Control' , IEEE Power and Energy Technology Systems Journal, Vol. 3, No. 2, PP 32-42, April 2016.

[41] H. Bawa, "ABB develops complete system solution for 1,100 kV HVDC power transmission." [Online]. Available: http://www.abb.com/cawp/seitp202/3a8302e9925218a4c1257d3f00451b52.aspx

[42] State Grid: Corporation of China, "Technology Specifications for ±1100 kV UHV DC Power Transmission Equipment Research Published." [Online]. Available: http://www.sgcc.com.cn/ywlm/mediacenter/corporatenews/05/247215.shtml

[43] Abd Almula G. M. Gebreel 'simulation and implementation of two level and three-level inverters by matlab and RT-lab' , master thesis , ohio State university , 2011

[44] Abd Almula G. M. Gebreel, Longya Xu 'Numerical Analysis and Simulation Implementation for SVPWM Based on a New Region Segment Configuration Method' , International Journal of Scientific & Engineering Research, Vol. 6, No. 3, PP 614-621, April 2015

[45] Abd Almula G. M. Gebreel, Longya Xu 'Power Conversion for UHVDC to UHVAC Based on Using MMC with Large Scale of Output Voltage Level' , International Journal of Electrical and Electronics Research, Vol. 4, No. 3, PP 125-139, April 2016

[46] Abd Almula G. M. Gebreel, Longya Xu 'DC–AC Power Conversion Based on Using Modular Multilevel Converter With Arm Energy Approximation Control' , IEEE Power and Energy Technology Systems Journal, Vol. 3, No. 2, PP 32-42, April 2016

[47] Abd Almula G. M. Gebreel, Longya Xu 'Power quality and total harmonic distortion response for MMC with increasing arm inductance based on closed loop-needless PID controller' , Electric Power Systems Research, Vol. 133, PP 281-291, April 2016

[48] Abd Almula G. M. Gebreel 'POWER CONVERSION FOR UHVDC TO UHVAC BASED ON USING MODULAR MULTILEVEL CONVERTER' , P.hD Dissertation, ohio State university , 2015

[49] Abd Almula G. M. Gebreel 'Survey on Topologies, and Control Techniques for the Most commom Multilevel Inverters' , International Journal of Scientific & Engineering Research, Vol. 6, No. 6, PP 345-353, June 2015

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